I claim:

1. A multiply unit comprising:

a first multiplier, a second multiplier, a third multiplier, and a fourth multiplier;

an adder having input ports which are larger than output ports of the multipliers, wherein an output port of the first multiplier is coupled to least significant bits of an input port of the adder, output ports of the second and third multipliers are coupled to input ports of the adder but not least or most significant bits of the input ports, and an output port of the fourth multiplier is coupled to an input port of the adder but not the least significant bits of the input port; and

an output circuit that provides output signals from the multipliers when the multiplier circuit operates in a first mode, and provides an output signal from the adder when the multiply unit operates in a second mode.

2. The multiplier of claim 1, wherein:

each multiplier is capable over multiplying an 8-bit value by an 8-bit value to generate a 16-bit result;

the first multiplier has an output port including 16 least significant bits coupled to 16 least significant bits of a first input port of the adder;

the second multiplier has an output port including 16 least significant bits coupled to bits eight through twenty-three of a second input port of the adder;

the third multiplier has an output port including 16 least significant bits coupled to bits eight through twenty-three of a third input port of the adder; and

the fourth multiplier has an output port including 16 least significant bits coupled to seventeen through thirty-two of a fourth input port of the adder.

3. The multiply unit of claim 1, further comprising an operand selection circuit coupled to the first, second, third, and fourth multipliers, wherein:

in the first mode, the operand selection circuit applies a first portion of a first operand signal and a first portion of a second operand signal to the first multiplier, applies a second portion of the first operand signal and a second portion of the second operand signal to the

second multiplier, applies a third portion of the first operand signal and a third portion of the second operand signal to the third multiplier, and applies a fourth portion of the first operand signal and a fourth portion of the second cperand signal to the fourth multiplier; and

in the second mode, the operand selection circuit applies the first portion of the first operand signal and the first portion of a second operand signal to the first multiplier, applies the second portion of the first operand signal and the first portion of the second operand signal to the second multiplier, applies the second portion of the first operand signal and the first portion of the second operand signal to the third multiplier, and applies the second portion of the first operand signal and the second portion of the second operand signal to the fourth multiplier.

4. A multiply unit comprising:

a first multiplier, a second multiplier, a third multiplier, and a fourth multiplier;

an adder coupled to the first, second, third, and fourth multipliers, wherein the first multiplier is connected so that a least significant bit output from the first multiplier corresponds to a least significant bit in the adder, the second and third multipliers are connected so that a least significant bit output from the second multiplier and a least significant bit output from the third multiplier correspond to a first bit that is more significant than the least significant bit of the adder, and the fourth multiplier is connected so that a least significant bit output from the fourth multiplier corresponds to a second bit that is more significant than the first bit in the adder; and

an output circuit that provides output signals from the multipliers when the multiplier circuit operates in a first mode, and provides an output signal from the adder when the multiply unit operates in a second mode.

5. The multiply unit of claim 4, further comprising latch circuits between the multipliers and the adder, the latch circuits latching the output signals of the multipliers so that the multipliers perform multiplication operations during a first clock cycle and the adder combines the output signals during a second clock cycle.

6. The multiplier of claim 4, further comprising operand selection logic coupled to the multipliers, wherein in the second mode, the operand selection logic separates a first

multiplicand into a first partial multiplicand and a second partial multiplicand, separates a second multiplicand into a third partial multiplicand and a second partial multiplicand, provides the first and third partial multiplicands to the first multiplier for multiplication, first and fourth partial multiplicands to the second multiplier for multiplication, second and third partial multiplicands to the third multiplier for multiplication, and second and fourth partial multiplicands to the fourth multiplier for multiplication.

7. The multiplier of claim 6, further comprising first and second two's complement units, each two's complement unit receiving a signed input value, wherein first and second two's complement unit respectively provides the first and second multiplicands representing absolute values of the respective signed input values.

8. The multiplier of claim 7, further comprising first, second, third, and fourth sign correction units coupled between the adder and the first, second, third, and fourth multipliers, respectively, the sign correction units operating to change or not sign of the output signal from the respective multipliers depending on a desired sign determined from the signed input values of the first and second two's complement units.

9. The multiply unit of claim 4, further comprising latch circuits between the adder and the first, second, third, and fourth sign correction units, the latch circuits latching the output signals of the sign correction units so that the multipliers and sign correction units perform multiplication operations during a first clock cycle and the adder combines the output signals during a second clock cycle.

10. A method for operating a multiply unit containing a plurality of multipliers, comprising:

operating the multipliers separately to generate a plurality of output product values when the multiply unit operates in a first mode; and

combining product values from the multipliers to generate only a single output product value when the multiply unit operates in a second mode.

11. The method of claim 10, wherein the output product values when the multiply unit operates in the first mode have a first data width that is one fourth of a data width that the single output product value has when the multiply unit operates in the second mode.

12. The method of claim 10, further comprising:

in the first mode, separating input data on a first input bus into a first, second, third, and fourth multiplicands; separating input data on a second input bus into fifth, sixth, seventh, and eighth multiplicands, and having first, second, third, and fourth of the multipliers respectively multiply the first and fifth multiplicands, the second and sixth multiplicands, the third and seventh multiplicands, the fourth and eight multiplicands; and

in the second mode, separating input data on the first input bus into a first and second multiplicands; separating input data on the second input bus into fifth and sixth multiplicands, and having first, second, third, and fourth of the multipliers respectively multiply the first and fifth multiplicands, the first and sixth multiplicands, the second and fifth multiplicands, the second and sixth multiplicands.